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A 5.7 GHZ VARIABLE-GAIN LOW NOISE AMPLIFIER (VGLNA) FOR LOW VOLTAGE APPLICATIONS

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RINGKASAN : *Satu topologi voltan rendah yang menggunakan elemen resonans berganding kapasitans telah diperkenalkan di dalam reka bentuk-reka bentuk dalam frekuensi radio (RF) yang kian mendesak. Topologi ini menggunakan skema penyahgandingan untuk mengasingkan secara dc, elemen litar yang bersambung secara sesiri dan berkongsi satu arus dc yang sama. Satu 5.7 GHz 0.18 μm CMOS amplifier yang bernilai haingar rendah dengan pembolehubah gandaan (VGLNA) telah digunakan untuk merealisasikan topologi ini. Hasil simulasi menunjukkan keputusan yang merangsangkan dengan VGLNA menunjukkan nilai hangar sebanyak 1.02 dB, kuasa gandaan sebanyak 19.41 dB, IIP3 bernilai -1.11 dBm dan julat penalaan gandaan sebanyak 6 dB. Penggunaan kuasa dilaporkan sebanyak 12.88 mW pada bekalan* V_{dd} *= 0.7 V. Satu perbandingan dilakukan antara VGLNA kaskod bervoltan rendah ini dengan VGLNA kaskod klasik. Keputusan perbandingan menunjukkan VGLNA kaskod bervoltan rendah ini mempersembahkan prestasi yang lebih baik.*

ABSTRACT : A low voltage topology that uses a capacitively coupled resonating element has been introduced in the ever demanding radio frequency (RF) designs. The topology utilises the decoupling scheme to dc isolate circuit elements that are connected in series and share a common dc current. A 5.7 GHz 0.18 μm CMOS variable-gain low noise amplifier (VGLNA) is used to realise the topology. Simulation shows promising results with the VGLNA exhibiting a noise figure of 1.02 dB, power gain of 19.41 dB, IIP3 of -1.11 dBm and gain tuning range of 6 dB. The power consumption reported is 12.88 mW at supply of V_{dd} = 0.7 V. A comparison is made between a low voltage cascode VGLNA and the classic cascode VGLNA. The results show that the low voltage cascode VGLNA performs better in most areas.

KEYWORDS : capacitively coupled, linearity, low voltage, power optimisation, variable-gain low noise amplifier

INTRODUCTION

With the emergence of potential markets for anytime, anywhere communications on a global basis, radio frequency (RF) design and implementation is in strong demand. Such demands have prompted many design challenges especially in low voltage and low power integrated circuits. Together with the bandwidth and sensitivity limitations, this goal calls for circuit and architecture breakthroughs.

Low supply voltage is one of the efficient methods to lower the circuit power consumption. The CMOS technology has the ability of operating at low supply voltages; 0.85-2.0 V (Shaeffer and Lee, 1997; Sullivan, Xavier *et al.,* 1997; Razavi, 1997; Nohra, Raut *et al.,* 2004). This paper presents a low-voltage topology for designing a variable gain low noise amplifier (VGLNA) operating at multi-giga Hertz applications. This topology uses capacitively coupled LC tanks.

LOW-VOLTAGE TOPOLOGY

Figure 1 is a widely used cascode LNA with source inductive degeneration. This amplifier requires two stacked transistors for stability purpose. The common gate MOSFET M2 can help reduce the Miller effect of the parasitic gate-drain capacitance of M1 (C_{gd1}). This allows one to do input matching easier. If each transistor has a threshold voltage of V_t, the absolute minimum supply voltage is 2Vt. For the conventional cascode amplifier, both dc and ac currents are shared between the two transistors. If the ac and dc portions of the circuit could be decoupled, the power supply voltage can be reduced.

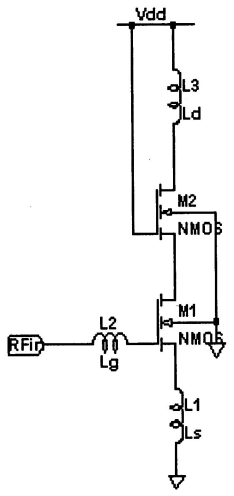

Figure 1. *Classic cascode LNA with source inductive degeneration structure*

In Figure 2, a low-voltage topology is illustrated for a VGLNA where the transistor M2 is folded to another biasing path and uses a coupling capacitor, C_{coup} to couple the RF signal. The scheme uses two on-chip LC tanks and one coupling capacitor. All LC tanks in the circuit are for matching purpose at the resonance operating frequency. At DC, the inductor provides a low resistance path for the Vdd to bias the two MOSFET individually. If the threshold voltage is V_t, the minimum required voltage supply in this circuit is only V_t, not $2V_t$. At radio frequency (RF) operation, the LC tanks have high impedance at resonance, so the tanks become open circuits and C_{coup} couples the RF signal. It works just like a traditional cascode LNA at the operating frequency.

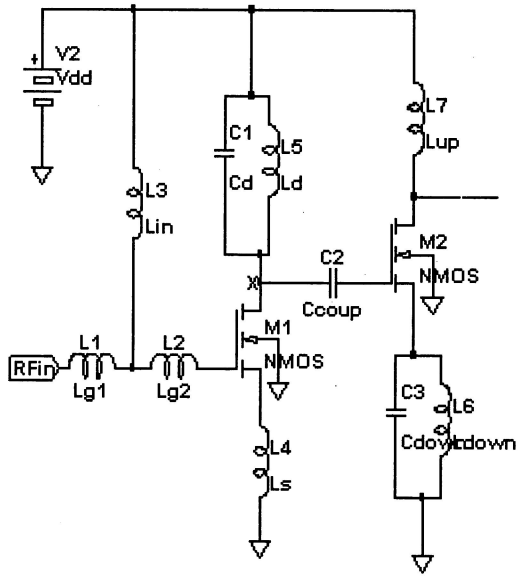

Figure 2. *Low voltage cascode LNA using decoupling scheme*

Since the coupling circuitry is isolated from the rest of the circuit, analysis would only be concentrated on this part. In Figure 3(a), an equivalent network representation of the coupling circuitry is shown. The equivalent resistance at resonance of the LC tanks is given by Manku and Beck (1998).

$$R_{rd} = (1 + Q^2)R_d \quad (1)$$

$$R_{rdown} = (1 + Q^2)R_{down} \quad (2)$$

where R_{rd} and R_{rdown} represent the series resistance for inductors L_d and L_{down} at frequency of operation respectively, and R_d and R_{down} denote the resistance of the LC_d and LC_{down} tanks at resonance. Figure 3(b) shows the network at the resonance condition. In order for the circuit to function adequately, it is required that Manku and Beck (1998)

$$R_{rd} \geq \left| \frac{1}{jw_0 C_{coup}} + \frac{R_{rdown}}{1 + g_{mdown} R_{rdown}} \right| \quad (3)$$

and

$$R_{rdown} \geq \frac{1}{g_{ds}}. \quad (4)$$

Using different values for the various components, the conditions for (3) and (4) can be satisfied to design a required circuit.

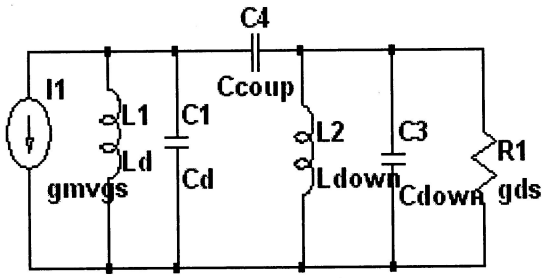

Figure 3(a). *Small signal circuit of the coupling elements.*

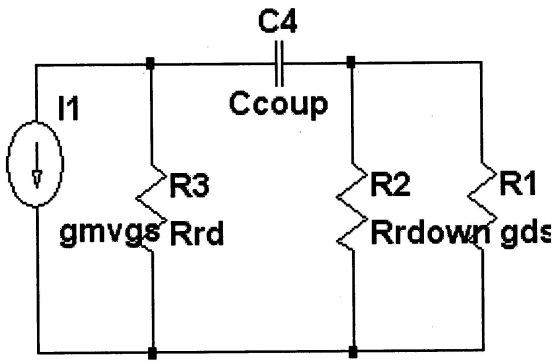

Figure 3(b). *Small signal circuit of the coupling elements at resonance.*

DECOUPLING SCHEME ON VGLNA

To verify the functionality of the low-voltage topology, a VGLNA is designed using the proposed structure and simulated. Figure 4 is the schematic for the VGLNA. The 0.18 μm CMOS process with RF model is used to simulate the circuit. The circuit is designed for 5.7 GHz Wireless Local Area Network (WLAN) frequency band. The VGLNA consists of two portions: the first is the low-noise cum decoupling stage and the second stage is the gain stage.

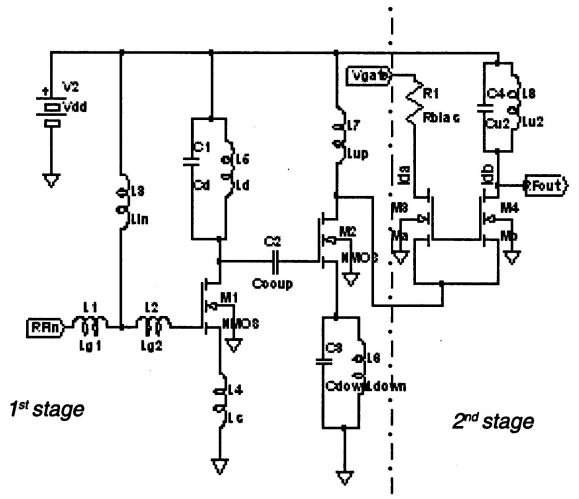

Figure 4. *Proposed VGLNA structure*

The transistors were chosen to bias at the operating frequency of 5.7 GHz. The gate-source voltage and drain-source voltage were all set equivalent to 0.7 V. The input matching is achieved by selecting L_g, L_s and the gate-to-source capacitance (C_{gs1}) of the transistor *M1*. The values of L_g and L_s were selected such that the input impedance to the amplifier equaled 50 ohm. Between the decoupling stage and the gain stage is a transistor *Mcas1* acting as a gain booster for the first stage and the *LC*-tank is for inter-stage matching network. The inter-stage matching network is designed to fit high frequency without degrading the noise performance of the circuit. Simulation result of the noise performance is shown in Figure 5; 1.02 dB.

The gain control is achieved by controlling the geometry ratio of transistors *Mb* and *Ma* in gain stage with the gate voltage, V_{gate} for both transistors remain unchanged. Based on the well-known drain current, I_d expression (Geiger, Allen *et al,* 1990),

$$I_d = \frac{1}{2}\,\mu_0 C_{ox}\,\frac{W}{L}\,(V_{gs} - V_{th})^2 \qquad (5)$$

the geometry ratio of the transistors influences the drain currents, I_{da} and I_{db}. Thus, a higher gain is possible by adjusting the width of the transistors. The *LC*-tank at this stage is used for output matching and a transistor at the output stage acts as a gain booster. The gain booster is fully matched to the output with the presence of *LC*-tank. Figure 6 shows the gain controllability through different geometry ratios for the transistors *Ma* and *Mb*. By keeping the length of the transistors constant, the widths, *Wb* and *Wa* are varied, providing the ratios of *Mb/Ma* ranging from 4 to 60.

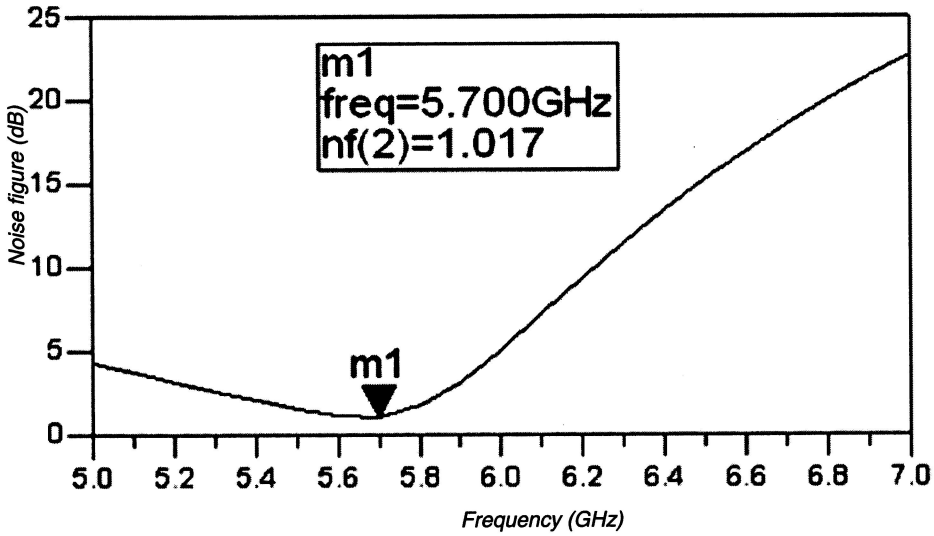

Figure 5. *Noise figure (NF) of the proposed VGLNA*

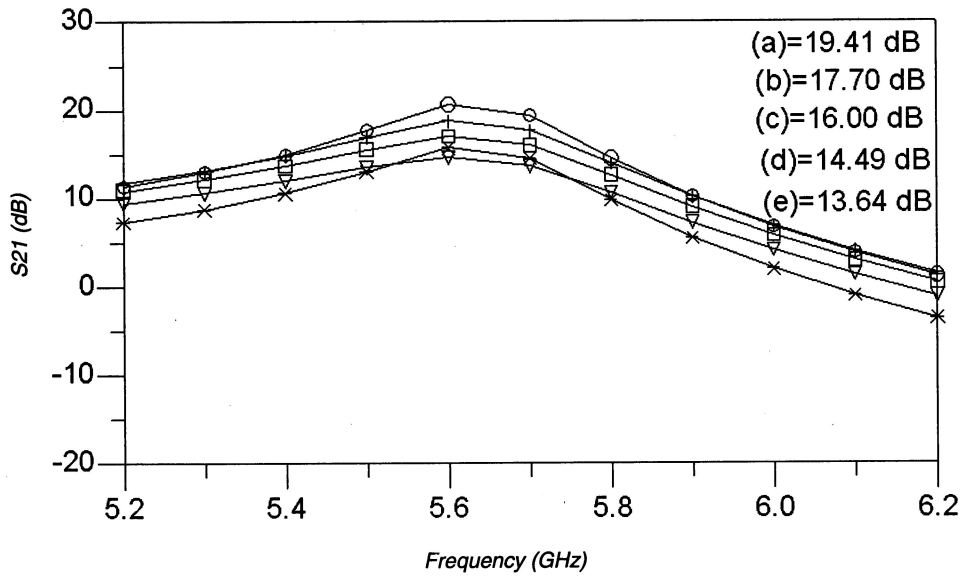

Figure 6. *Variable gain performance in different geometry ratios*

Figure 7 is the power gain (S21) and the input reflection coefficient (S11) of the VGLNA with 0.7 V supply. As shown in Figure 7, the S21 and S11 resonate at the operating frequency with both upper and lower peaks resonating at resonance frequency of 5.7 GHz. The optimised power gain, S21 should be as high as possible and it is simulated as 19.4 dB. As for the input reflection coefficient, S11 is desired to be less than -12 dB and in this proposed design; the S11 is equivalent to -13.5 dB. The invert gain, S12 is -87.8 dB and the output reflection

coefficient, S22 is -23.0 dB. The noise figure (NF) as reported in Figure 5 is 1.02 dB at 5.7 GHz. The value of IIP3 simulated is equivalent to -1.11 dBm. Table I shows a comparison made between proposed cascode VGLNA (Figure 4) optimised for linearity and power with a traditional 1.8 V cascode amplifier topology (Liao and Chuang, 2003). For the comparison, both designs have been chosen to operate at WLAN frequency band and were tuned to operate at its tradeoffs between linearity, noise and power matching. The main difference is the structure of the design for the use of the capacitively coupled resonating element in the low voltage topology.

From Table I, we note that the low voltage cascode VGLNA has shown significant improvement of performance in most areas especially in noise figure and power gain. There is significant

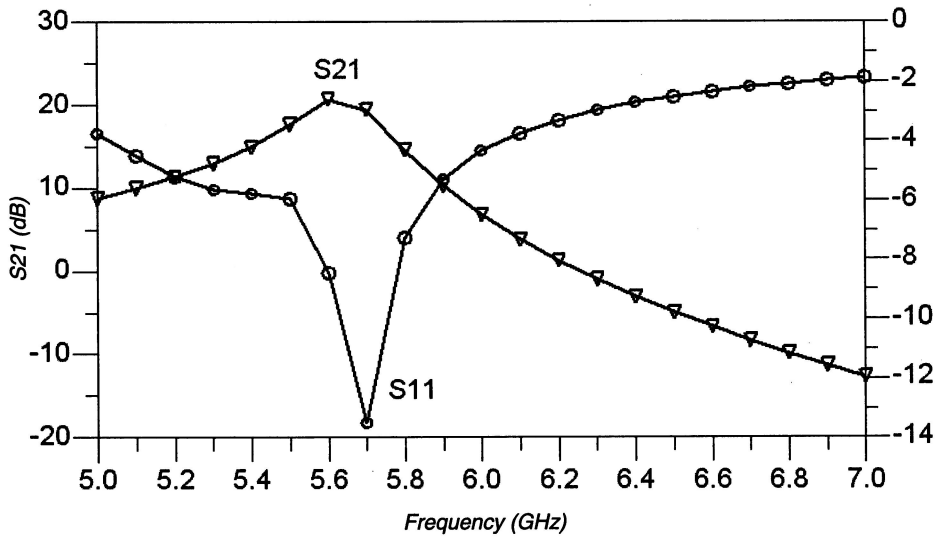

Figure 7. *S21 and S11 of the proposed VGLNA*

tradeoff between power consumption and linearity. One low voltage cascode has been optimised for linearity by making sure its stability with reasonable S11, S22 and IIP3. On the other hand, the same low voltage cascode which has been optimised for power shows that there is 6.79 dB improvement in power consumption and this is with tradeoff of linearity or stability; S11, S22 and IIP3. The low voltage cascode shows an enhanced noise figure (NF) of 2.6 dB compared to traditional cascode. This enhancement is due to the fact that some of the shot noise associated with *M2* has been diverted to ground by the capacitively coupled resonating elements and does not enter *M1*. This helped to reduce the noise figure, increase linearity or both.

Table 1. Comparison between a traditional gascose amplifier and the proposed low voltage VGLNA

Parameters	Proposed Low Voltage Cascode		Traditional Cascode topology (Liao and Chuang, 2003)
	Linearity	Power	
Supply voltage (V)	0.7	0.7	1.8
Power (mW)	19.67	12.88	72.1
Operating frequency (GHz)	5.7	5.7	5.7
Noise figures (dB)	1.02	1.13	3.76
Gain (dB)	19.42	15.51	11.20
S11 (dB)	-13.52	-13.48	-18.63
S22 (dB)	-22.98	-1.43	-16.99
IIP3 (dB)	-1.11	-6.01	0.70
Gain variation (dB)	6	6	5

CONCLUSION

The low voltage topology VGLNA is presented in this paper. The basic criteria for implementation of the circuit have been outlined. The supply is only 0.7 V and the performance of the circuit is still desirable. A comparison was made between conventional cascode VGLNA working at 1.8 V and the new low voltage cascode VGLNA at 0.7 V. The comparison showed that the low voltage cascode VGLNA had better noise performance and improved power consumption compared to the conventional cascode VGLNA.

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